What is claimed are:

1. A method of forming an isolation film in semiconductor devices, comprising the steps of:

forming a mask pattern on a silicon substrate in a memory cell region and a peripheral circuit region and then etching an exposed portion of the silicon substrate by a given depth to form a shallow trench;

implanting an inert ion into the surface of the trench in the peripheral circuit region;

implementing an oxidization process so that an oxide film is grown on the surfaces of the trenches in the memory cell region and the peripheral circuit region, wherein the depth of the trench in the peripheral circuit region is increased due to excessive oxidization at the portion in which the ion is implanted; and

forming an oxide film on the entire structure so that the trench is buried and planarizing the surface of the oxide film.

2. The method as claimed in claim 1, wherein the mask pattern consists of a pad oxide film and a pad nitride film.

3. The method as claimed in claim 1, wherein the trenches have sidewalls having a tilt angle of 80 ~ 85° .

4. The method as claimed in claim 1, wherein the inert ion is entire silicon (Si) or argon (Ar).

5. The method as claimed in claim 4, wherein the silicon (Si) ion is implanted with energy of 5 ~ 50KeV at the dose of 1E13 ~ 1E16cm^{-2}.

6. The method as claimed in claim 4, wherein the argon (Ar) ion is implanted with energy of 5 ~ 50KeV at the dose of 1E14 ~ 1E16cm^{-2}.

7. The method as claimed in claim 1, wherein the oxidization process is implemented at a temperature of 800 ~ 1100℃ to a target thickness of 30 ~ 150Å.

8. The method as claimed in claim 1, wherein the planarization is performed by means of a chemical mechanical polishing method.

9. A method of forming an isolation film in semiconductor devices, comprising the steps of:

forming a mask pattern on a silicon substrate in a memory cell region and a peripheral circuit region and then etching an exposed portion of the silicon substrate by a given depth to form a shallow trench;

implanting an inert ion into the surface of the trench in the peripheral circuit region;

performing a rapid thermal oxidization process in order to an anti-diffusion layer is formed at the bottom of the trench

implementing an oxidization process so that an oxide film is grown on the surfaces of the trenches in the memory cell region and the peripheral

circuit region, wherein the depth of the trench in the peripheral circuit region is increased due to excessive oxidization at the portion in which the ion is implanted; and

forming an oxide film on the entire structure so that the trench is buried and planarizing the surface of the oxide film.

10. The method as claimed in claim 9, wherein the mask pattern consists of a pad oxide film and a pad nitride film.

11. The method as claimed in claim 9, wherein the trenches have sidewalls having a tilt angle of 80 ~ 85° .

12. The method as claimed in claim 9, wherein the inert ion is entire silicon (Si) or argon (Ar).

13. The method as claimed in claim 12, wherein the silicon (Si) ion is implanted with energy of 5 ~ 50KeV at the dose of 1E13 ~ 1E16cm^{-2}.

14. The method as claimed in claim 12, wherein the argon (Ar) ion is implanted with energy of 5 ~ 50KeV at the dose of 1E14 ~ 1E16cm^{-2}.

15. The method as claimed in claim 9, wherein the rapid thermal oxidization process is performed by means of a spike annealing process.

16. The method as claimed in claim 15, wherein the spike annealing process is implemented at a temperature of 850 ~ 1100℃ and the ramp-up ratio is controlled to be 100 ~ 250℃ /sec.

17. The method as claimed in claim 9, wherein the oxidization process is implemented at a temperature of 800 ~ 1100℃ to a target thickness of 30 ~ 150 Å.

18. The method as claimed in claim 9, wherein the planarization is performed by means of a chemical mechanical polishing method.